24.7 Two 10Gb/s/pin Low-Power Interconnect Methods for 3D ICs

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Three-dimensional integrated-circuit (3DIC) technology has received growing recognition in recent years for possibly overcoming fundamental limitations imposed by the conventional 2-dimensional planar IC (2DIC) technologies. The 3DIC offers significant advantages over the 2DIC in performance, integrated functionality, and form factor. With the multiple tiers of active device layers stacked upon each other in the third dimension, it can potentially reduce the communication latency among various functional tiers (for instance: microprocessors, memories, mixed-signal circuits, and RF/wireless I/Os, as shown in Fig. 24.7.1(a) and boost the switching speed and analog bandwidth of the overall integrated system with reduced power consumption, increased packing density, and decreased packaging size, weight, and cost. The 3DIC also opens possible avenues for heterogeneous integration among Si, SiGe, and GaAs or InP IC technologies in different tiers of active device layers without facing technology and manufacturing incompatibilities and cross-contamination issues. However, despite the above mentioned potential system merits, the vertical interconnects among active device layers have been identified as one of the major technical difficulties that hinder the 3DIC manufacturing yield and circuit performance [1].

Unlike the direct-contact inter-tier interconnection method, contactless interconnect methods by using either inductive- [2, 3] or capacitive-coupling [4] principles have been proposed in the past to facilitate inter-tier communications in 3DIC. Both contactless methods, shown in Fig. 24.7.1(c)(d), have advantages over the direct-contact interconnect, shown in Fig. 24.7.1(b), in terms of relaxed overlay alignments and less processing complexity without the use of vertical vias and studs. By using subsequent wafer bonding techniques [1], the contactless interconnects can lead to higher yield, lower cost, and higher reliability in 3DIC production with multiple active device tiers made of various IC technologies.

For longer-distance inter-chip (or inter-tier) communications, the inductive signal coupling can be more efficient since it exploits magnetic flux that is detectable from several hundreds of microns away. However, the inductive-coupling method has 2 primary disadvantages: it demands large inductor size (~100×100μm^2) and can cause serious crosstalks.

When the inter-tier communication distance is reduced to several microns like that in 3DIC, the electrical coupling via capacitors is superior due to a more confined electrical field that induces less crosstalk among vertical communication pins. In this case, a moderate size of capacitor (~28×28μm^2) can provide sufficient capacitance (~9fF) to enable the vertical signal coupling between adjacent tiers with 3μm distance. Only a moderate adjacent pin distance of 19.5μm (6.5× of the inter-tier distance in 3DIC) is required to achieve the desired 1×10^{-12} BER.

Two capacitive coupling methods are used in creating low-power and high-bandwidth vertical (inter-tier) interconnects in 3DIC: UWB impulse-shaping interconnect (UII) and RF interconnect (RFI). Both interconnects are implemented in MIT-Lincoln Lab 0.18μm CMOS 3DIC to realize 10Gb/s/pin and 11Gb/s/pin transmission bandwidths, respectively, with 2.7mW/pin and 4.35mW/pin power consumption. Compared with previous works [2-4], these 2 interconnects have advanced the state-of-the-art in both efficiency (with 0.27pJ/b and 0.39pJ/b, respectively) and data rates (>10Gb/s/pin).

Figure 24.7.2(a) shows the proposed UlI scheme. Traditional impulse UWB (I-UWB) system modulates baseband signals into impulses. And the receiver conducts timing correlation and signal recovery. Due to the relatively short distance in 3DIC vertical communication, the receiver does not require a sophisticated ADC or a complicated correlator, but rather it uses a high-sensitivity impulse recovery circuit to retrieve the transmitted baseband signals from injected impulse series. As shown in Fig. 24.7.3, a low-swing pulse sense amplifier is used to recover input impulse series into the NRZ baseband sequence. Due to the speed constraint and device mismatch, this sense amplifier can only recover over-35mV$_{pp}$ signal with 20ps impulse-width in 0.18μm CMOS. A resistor-biased complementary LNA , shown in Fig. 24.7.3(a), is inserted to increase the receiver sensitivity by 8.5dB (or to 13.2mV$_{pp}$) and help halve the coupling capacitor size with the same performance.

In the traditional I-UWB system, impulse width is precisely controlled by a power-hungry DLL and an impulse modulator to facilitate high-speed transmission with ultra-wide spectrum. In the proposed UII system, the coupling capacitor is designed jointly with the LNA input resistance to confine the impulse-width at about 1/4-period of the highest data rate to maintain the receiver sensitivity and avoid the possible ISI. Based on simulation, the UII scheme functions well up to 30% of variation in impulse width, which can tolerate typical Foundry RC process variations on the wafer. Although a smaller coupling capacitor is preferred for the purpose of cost and energy savings, its size is determined according to the signal strength, receiver sensitivity, and required system BER, as shown in Fig. 24.7.3(b). Calculation shows that a coupling capacitor >7.3fF is sufficient for achieving the desired 10^{-12} BER under 1V supply, which corresponds to a minimum 44×14μm^2 chip area with 3μm inter-tier distance. Given a 2μm alignment margin on each side, a 48×18μm^2 coupling capacitor is thus used.

The other proposed 3D interconnect is RFI, as shown in Fig. 24.7.2(b). The NRZ baseband signal is upconverted by an RF carrier using the ASK modulation. An RF envelope detector in the RX charges/discharges the sense-amplifier input capacitor according to the NRZ input. Figure 24.7.4 shows the RFI TX/RX circuit. A differential complimentary passive mixer is used in the TX to modulate NRZ data into ASK signal and a mixer is designed as the RF envelope detector to convert received ASK signal into NRZ data. In contrast to conventional RF systems, this RFI is self-synchronized and does not need extra frequency/phase synchronization or extraction of accurate carrier frequency, which greatly relaxes the transceiver system complexity.

The choice of RF carrier frequency is affected by the RF envelope detector charging/discharging speed and the signal data rate. With device f_T limitation of 0.18μm CMOS technology, the optimum carrier frequency for 10Gb/s RFI is 20 to 30GHz. As in the UII system, the coupling-capacitor size is also determined by the signal strength, receiver sensitivity, and system BER. Given the 1V supply and the 25GHz RF carrier, 27.3fF/81.9fF coupling capacitance are needed to accomplish 10^{-12} BER for N/P differential branches, with minimum 68×34μm^2/112×62μm^2 chip areas, respectively. In the RFI prototype, 72×38μm^2/116×66μm^2 capacitors are actually used to allow 2μm alignment margin on each side.

With their unique characteristics, UII and RFI are instrumental for different applications. UII is suitable for low-power design, but RFI is more robust in a high switching-noise (or interference) environment. As shown in Fig. 24.7.5, the measured data rates for UII and RFI are 10Gb/s/pin and 11Gb/s/pin, respectively, with power consumption of 2.7mW/pin and 4.35mW/pin. The added rms jitters are measured as 0.88ps and 0.49ps, respectively, for UII and RFI. The BERs for both interconnects are measured to be $<1.02\times10^{-14}$ by using 2^{31}-1 PRBS from the Agilent-71612. Figure 24.7.6 summarizes the performance of UII and RFI in both speed and energy efficiency (0.27pJ/b and 0.39pJ/b, respectively), which are at least 6× superior to prior arts based on either capacitor- or inductor-coupled vertical interconnects for 3DIC applications [2-4]. The 3DIC die micrographs are shown in Fig. 24.7.7. The active chip area is 0.0012mm^2 for UII interconnects and 0.0021mm^2 for RFI interconnects.

Acknowledgements:
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References:
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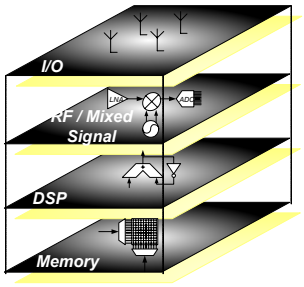
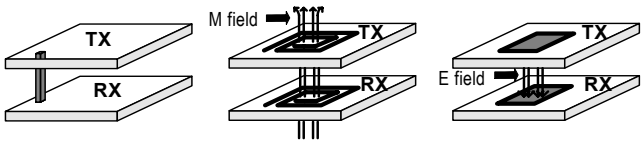
[2] D. Mizoguchi, Y. B. Yusof, N. Miura, et al., "A 1.2Gb/s/pin Wireless Superconnect Based on Inductive Inter-Chip Signaling (IIS)," *ISSCC Dig. Tech. Papers*, pp.142-143, Feb., 2004.
[3] A. Iwata, M. Sasaki, T. Kikkawa, et al., "A 3D Integration Scheme Utilizing Wireless Interconnections for Implementing Hyper Brains," *ISSCC Dig. Tech. Papers*, pp. 262-263, Feb., 2005.
[4] K. Kanda, D. D. Antono, K. Ishida, et al., "1.27Gb/s/pin 3mW/pin Wireless Superconnect (WSC) Interface Scheme," *ISSCC Dig. Tech. Papers*, pp. 186-187, Feb., 2003.

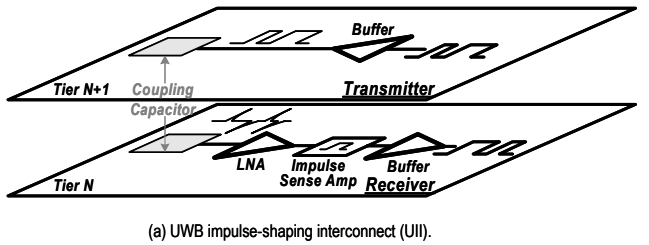


(a) 3DIC technology.

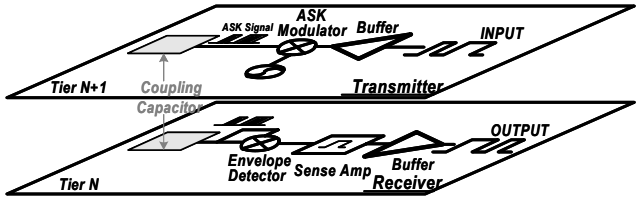


(b) Direct contact. (c) Inductor coupling. (d) Capacitor coupling.

Figure 24.7.1: (a) 3DIC and (b)-(d) inter-tier interconnects between active device layers.

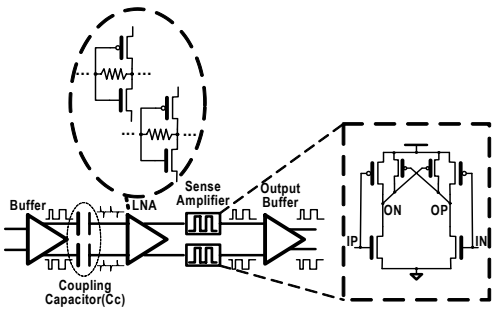


(a) UWB impulse-shaping interconnect (UII).

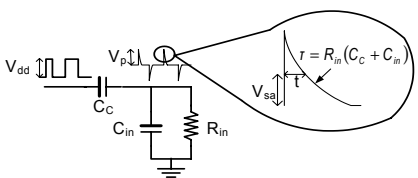


(b) RF Interconnect (RFI).

Figure 24.7.2: UII and RFI vertical interconnects for 3DIC.



(a) Signal recovery circuit in UII.



(b) Design consideration of coupling capacitor and equivalent model.

Figure 24.7.3: UII Circuit (a) design and (b) analysis.

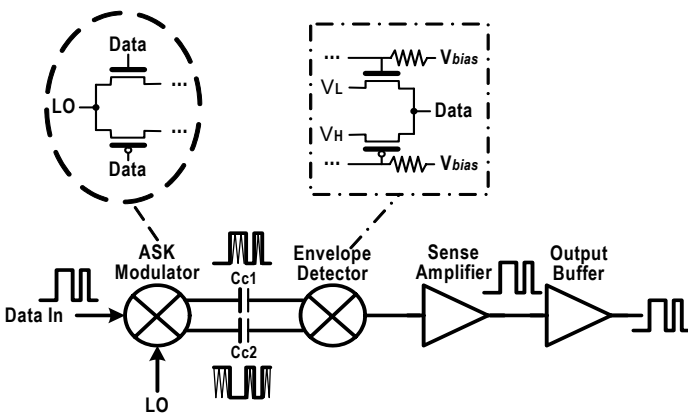
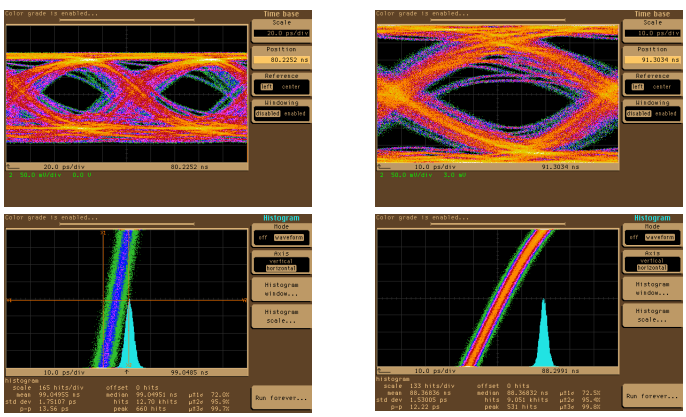


Figure 24.7.4: ASK Modulator and Envelope Detector in RFI.



(a) UII tested at 10Gb/s with added jitter: 0.88ps$_{rms}$

(b) RFI tested at 11Gb/s with added jitter: 0.49ps$_{rms}$

Figure 24.7.5: Output-signal eye-diagram and jitter measurements for UII and RFI.

	Kanda, 2003 ISSCC	Mizoguchi, 2004 ISSCC	Iwata, 2005 ISSCC	This Work	
				UII	RFI
Contactless Method	Capacitive	Inductive	Inductive	Capacitive	Capacitive
Technology	2D 0.35μm CMOS	2D 0.35μm CMOS	2D 0.25μm CMOS	3D 0.18μm CMOS	3D 0.18μm CMOS
Carrier	Baseband	Baseband	Baseband	Baseband	25GHz
Supply	3.3V	3.3V	2.5V	1.0V	1.0V
Speed	1.27Gb/s	1.2Gb/s	800Mb/s	**10Gb/s**	**11Gb/s**
Energy/bit	2.4pJ/b	38pJ/b	11.3pJ/b	**0.27pJ/b**	**0.39pJ/b**
Power	3mW	45.5mW	9mW	2.7mW*	4.3mW*
Active Chip Area	0.0005mm^2	0.0044mm^2	N/A	0.0012mm^2	0.0021mm^2
BER	N/A	N/A	N/A	**<1.02x10^{-14}**	**<1.02x10^{-14}**

* The power consumptions do not include buffer.

Figure 24.7.6: UII and RFI performance summary and comparison with prior arts.

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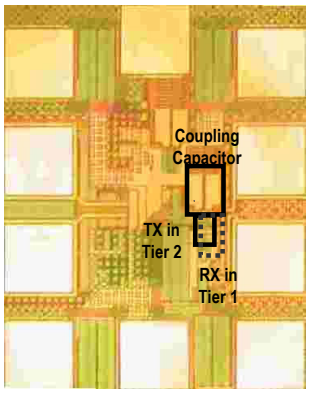
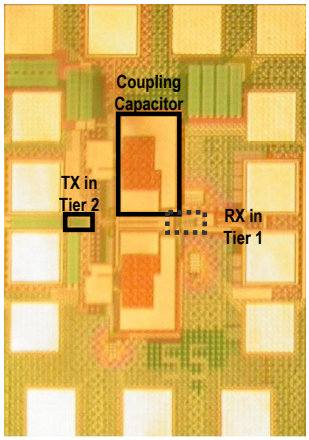


(a) UII 3DIC.



(b) RFI 3DIC.

Figure 24.7.7: 3DIC die micrographs for UII and RFI.

